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DEVICE AND PROCESS FOR ADJUSTMENT OF AN OPERATING PARAMETER OF AN ANALOG ELECTRONIC CIRCUIT

PRIORITY CLAIM

The present application claims priority from French Application for Patent No. 02 09615 filed July 29, 2002, the disclosure of which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

Technical Field of the Invention

[1] The present invention relates to the domain of analog electronic circuits. More particularly, the invention relates to a device and a process for adjustment

of an operating parameter of such a circuit. One particularly attractive application of such a device and such a process relates to the adjustment of the reference voltage supplied by a reference voltage source.

Description of Related Art

[2] A reference voltage source is an analog circuit that outputs a constant voltage independent of the operating temperature and the applied power supply current.

[3] As it is conceived, the value of the voltage output by the reference voltage source is a parameter that has to be fixed very precisely. However during assembly, and particularly when the circuit is packaged, the voltage output by the circuit may drift significantly.

[4] Reference voltage sources are provided with an adjustment device, for example a device integrated into one of the stages of the source, to compensate for this drift. This adjustment device acts by adapting the global value of resistances placed between the anode and the cathode of the circuit as a function of the voltage to be adjusted, using fusible elements that can be selectively activated.

[5] The voltage output by the analog circuit is adjusted by selecting one or several fusible elements and

by applying a sufficiently high voltage to these elements so that they break down.

[6] These fusible elements are selected and activated using specific pins, each of which communicates with one of the fusible elements.

[7] Thus, electronic circuits of this type do not have a standard configuration, to the extent that they include additional pins.

[8] Furthermore, the parameter is adjusted before packaging, in other words before the parameter to be adjusted is affected by a drift. Therefore, this adjustment is made in advance and is necessarily imperfect.

[9] There is a need to overcome these disadvantages and to provide a device and a method for adjusting an operating parameter of an analog circuit that can be integrated into a standard analog circuit and that is capable of compensating for the drift of the parameter during packaging, with improved precision.

SUMMARY OF THE INVENTION

[10] The present invention proposes a device for the adjustment of an operating parameter of an analog

electronic circuit. A set of adjustment resistances can be configured from outside the circuit to modulate the value of resistances in the circuit and thus adjust the value of the said parameter. Fusible means are provide associated with one of the said adjustment resistances and that will be selected and activated to configure the resistances of the adjustment device.

[11] According to one general feature of this adjustment device, it also includes a combinational logic circuit that receives a control signal as input applied from outside the circuit onto a terminal of this circuit and adapted to select one of the fusible means as a function of a signal applied to it.

[12] According to another special feature of this device, it comprises a count circuit connected to the logic circuit and to which the control signal is applied as input, to increment the count in the count circuit forming an addressing signal of the fusible means, at each transition of this control signal.

[13] It also comprises a circuit for controlling activation and de-activation of the electronic circuit and the adjustment device connected between the said terminal of the circuit and the count circuit and comprising a stage to control activation and de-activation of the electronic circuit and a stage to generate a clock signal controlling the count circuit.

[14] According to one embodiment, each control stage comprises a set of diodes in series connected between the said terminal of the analog electrical circuit and a switching element controlled as a function of the voltage applied to the said terminal of the circuit, the said diodes jointly defining a threshold voltage for activation of the switching element.

[15] According to one embodiment, each control stage is provided with a hysteresis circuit.

[16] According to one specific feature of the count circuit, the count circuit comprises a set of count flip flops and a set of logical gates at the input to the count circuit so as to accelerate transitions of the control signal.

[17] For example, the adjustment resistances are arranged in series with the corresponding fusible elements, with each assembly being composed of an adjustment resistance and a fusible element being arranged in parallel on a resistance of this circuit to be adjusted.

[18] According to another specific feature of the device according to the invention, each of the fusible elements is formed from a MOS transistor with a parasite two-pole transistor.

[19] According to one advantageous embodiment, it comprises means of adjusting a breakdown voltage threshold of the fusible elements.

[20] For example, these adjustment means may comprise a resistance bridge arranged between the grid and the source and between the grid and the drain of each MOS transistor.

[21] The invention also proposes an analog electronic circuit, for example a reference voltage source, which comprises an adjustment device like that defined above.

[22] The invention also proposes a process for adjustment of an operating parameter of an analog electronic circuit, comprising a set of adjustment

resistances configurable from the outside of the circuit to modulate the value of circuit resistances and thus to adjust the value of the said parameter, and fusible means each associated with one of the said adjustment resistances and that will be selected and activated to configure the resistances of the adjustment device, this process being designed for use with an adjustment device like that defined above.

[23] This process comprises the following steps:

- measure the circuit operating parameter;
- set a count circuit to zero;
- set the circuit power supply voltage above a first threshold value so as to de-activate the circuit;
- generate a device control clock signal so as to increment the count circuit to a count level corresponding to one of the fusible means;
- decode the clock signal and select the corresponding fusible means; and
- increase the level of the power supply voltage up to the breakdown voltage of the fusible means.

BRIEF DESCRIPTION OF THE DRAWINGS

[24] A more complete understanding of the method and apparatus of the present invention may be acquired by reference to the following Detailed Description when taken in conjunction with the accompanying Drawings wherein:

[25] FIGURE 1 is a block diagram illustrating the structure of an adjustment device according to the invention;

[26] FIGURE 2 is an example of a time diagram showing the variation of the control signal Vc applied to the cathode of the reference voltage source, as a function of time;

[27] FIGURE 3 is a diagram illustrating the structure of the activation and de-activation control circuit for the electronic circuit and the adjustment device;

[28] FIGURES 4a and 4b are detailed views of the circuit in FIGURE 3, illustrating the hysteresis circuit;

[29] FIGURE 5 shows curves illustrating the behavior of the activation and de-activation control circuit in FIGURE 3;

[30] FIGURE 6 is a diagram illustrating the structure of the count circuit;

[31] FIGURE 7 is a diagram illustrating the composition of the combinational logic circuit;

[32] FIGURE 8 is a truth table that generates the combinational logic circuit;

[33] FIGURES 8a and 8b show the structure of the fusible means selection circuit;

[34] FIGURE 9 illustrates the composition of the fusible means used to modulate the resistance values of the analog electronic circuit; and

[35] FIGURE 10 is a general diagram showing the selection and activation stage of the fusible elements.

DETAILED DESCRIPTION OF THE DRAWINGS

[36] FIGURE 1 shows the general structure of a device for adjustment of an operating parameter of an analog electronic circuit, denoted by the general numeric reference 10.

[37] In the example embodiment shown, this adjustment device is designed to adjust the reference voltage supplied by a reference voltage source, which must output a fixed voltage independently of its operating temperature or its power supply current.

[38] The invention could also be equally applicable to any type of analog electronic circuit for which an operating parameter has to be precisely adjusted, independently of its operating conditions, such as an operational amplifier or a comparator for which the output voltage must be precisely defined, or an oscillator for which the frequency has to be precisely adjusted, etc.

[39] As can be seen in FIGURE 1, the adjustment device 10 will be placed in parallel on a stage 12 of the reference voltage source, which comprises a resistive bridge composed of resistances R_A, R_B, R_C and R_1, R_2 associated with a transistor Q, the assembly being connected between a cathode C and an anode A that form the external terminals of the reference voltage source.

[40] More particularly, the adjustment device 10 is arranged in parallel on some of the resistances, denoted as numeric references R_1 and R_2, in order to modulate their resistance value to adjust the reference voltage output by the source, so as to correct the drifts generated during assembly of the circuit by modulating the global value of the resistive bridge between the anode and the cathode.

[41] The adjustment device 10 essentially comprises an activation and de-activation control circuit 14 for the source 12 and the adjustment circuit 10 that is connected to the cathode C; a count circuit 16 connected to the activation and de-activation control circuit 14, that will be incremented on each transition of a control signal visible in FIGURE 2; a combinational logic circuit 18 that decodes the output from the count circuit 16; a network of fusible elements 20 that can be selectively activated under the control of the logic circuit 18 as a function of the output from the count circuit 16; and a modulation stage 22 modulating resistances R_1 and R_2 composed of a set of variable resistances each placed in series with a fusible element in the fuses network 20 and in parallel on one of the resistances R_1 and R_2 to be adjusted.

[42] As can be seen in this FIGURE 1, the adjustment device 10 is connected between the cathode C and the resistances R_1 and R_2. Thus, it uses standard pins of the voltage source and can operate without the need for any special pins. The control signal applied to the cathode of the source is a means firstly of selecting fusible elements and adjustment resistances for resistances R_1 and

R_2, and secondly of provoking the selective connection of adjustment resistances in parallel on resistances R_1 and R_2 by taking action on fusible elements, external to the circuit, after packaging.

[43] As it is conceived, during operation of the reference voltage source, the adjustment device 10 must be inactive. In this case, a current is injected through the cathode C that outputs a constant voltage called the "reference" voltage. On the other hand, in reference voltage adjustment mode, the adjustment device 10 must be active and the reference voltage source 12 must be inactive. The cathode C is then used as the power supply for the adjustment device.

[44] Also with reference to FIGURE 2, the operating principle for this adjustment device is as follows. For a power supply voltage applied to the cathode C less than a first threshold voltage UVLO2 (Under Voltage Lock out 2), the adjustment device 10 is inactive, the output from the count circuit 16 is equal to zero and the fusible elements in network 20 are inactive, in other words they are conducting. If the power supply voltage exceeds this first threshold value UVLO2, the output stage of the reference

voltage source is disabled and the adjustment device 10 is activated. In order to select the fusible elements of the fuses network 20 and the corresponding adjustment resistances of stage 22, a clock circuit is generated around a power supply voltage UVLO1 that increments the count circuit 16. The counter level is then defined by the number of clock periods completed. This number of periods is then decoded by the combinational logic circuit 18 so that one or several fusible elements and the corresponding resistances can be selected. Once the fusible element has been selected, the voltage of cathode C is increased until the breakdown voltage of the fusible element. Thus, the value of the resistances R_1 or R_2 is modified to adjust the voltage output by the reference voltage source accordingly.

[45] When the reference voltage has thus been adjusted in this manner, the circuit may be used as the reference voltage source.

[46] As will be described later, steps will be taken to prevent the activation voltage of fusible elements in the fuses network 20 from being greater than the maximum allowable voltage depending on the technology used by the voltage source, in order to avoid damaging the circuit.

[47] We will now describe the structure of the activation and de-activation control circuit for the reference voltage source of the adjustment device 10, with reference to FIGURE 3. This control circuit 14 performs two functions. The first function is to inhibit the adjustment device during normal operation of the reference voltage source and to set the count circuit to zero. The second function is to format the control signal, in other words the clock signal applied to the count circuit.

[48] As can be seen in FIGURE 3, the activation and de-activation control circuit 14 comprises a first stage 24 that generates the clock signal H that will be used in the count circuit, and a second activation and de-activation control stage 26 of the reference voltage source, that outputs the first threshold value UVLO2.

[49] Each of these stages comprises a set of diodes, composed of the p-n junctions of the two-pole transistors, namely T1, T2 and T3, T4, T5, T6 and T7; and T8, T9, T10, T11 respectively.

[50] Concerning the network of diodes T1 to T7 in the first stage 24, they are connected to the cathode C and to the ground through a resistance R3. The two-pole

transistor T6 forming one of the diodes in the diodes network is connected to a grid G of a transistor M1 through a first hysteresis circuit 30, the drain D of this MOS transistor M1 outputting the clock signal H through a second hysteresis circuit 32.

[51] Similarly, diodes T8 to T11 in the second stage 26 are connected firstly to the cathode C and secondly to the ground through a resistance R4. The common terminal between the transistor T11 and the resistance R4 is connected to the grid G of a MOS transistor M2. The drain D of this MOS transistor M2 is connected to a node U2, which outputs the threshold voltage UVLO2 through an inverter gate 28.

[52] This circuit 14 operates as follows.

[53] When the power supply voltage applied to the cathode C is less than the threshold voltage UVLO2, the network of diodes composed of transistors T8 to T11 is blocked. The transistor grid M2 is then connected to the ground through the resistance R4. The voltage of node U2 is then at a high level, and the output from the inverter gate 28 is at a low level. This voltage then controls the count circuit 16 through an appropriate conventional type

of stage, so as to reset the counters in the circuit to 0. The adjustment device is then inactive. For a power supply voltage greater than the threshold voltage UVLO2, the diodes composed of transistors T8 to T11 are conducting. The MOS transistor M2 that operates under saturated conditions, connects node U2 to the ground. The device is then active and the reference voltage source is deactivated.

[54] Furthermore, when the power supply voltage output to the cathode C is less than the voltage level UVLO1, the diodes formed by transistors T1 to T7 are not conducting. The grid G of transistor M1 is made high through a MOS transistor M3 placed between the cathode and the anode, the grid of which is connected to the common node between the transistor T7 and the resistance R3 and that operates under non-conducting conditions. The node U1 is then set to a high level.

[55] If the power supply voltage is greater than the voltage UVLO1, the diodes formed by transistors T1 to T7 are conducting. The transistor M3 that operates under linear conditions connects node U1 to the ground. The counter is then incremented.

[56] As mentioned above, hysteresis circuits 30 and 32 are used to create a hysteresis in operation of this control circuit 14, as can be seen in FIGURE 5.

[57] The hysteresis circuit 30 associated with the first stage 24 comprises a MOS transistor M4 associated with one of the diodes, namely the diode composed of the two-pole transistor T6, and an inverter switch 34 placed between the node U1 and the MOS transistor M4.

[58] Thus, with this arrangement, the node U1 switches from the high level to the low level when all diodes T1 to T7 are conducting. On the other hand, it will change from the low level to the high level when diodes denoted T1 to T6 are conducting, in other words for a lower power supply voltage. When node U1 is at a low level, the MOS transistor M4 is conducting, the diode denoted by the reference T6 is short circuited, which means that U1 will change to a lower voltage. This hysteresis was created to overcome a possible variation due to the noise present on the power supply voltage that generates the counter clock signal, which could generate count errors within the count circuit 16.

[59] FIGURE 4a and 4b show a similar circuit 32 that is also used to generate a hysteresis. On these diagrams, the elements of the circuit in FIGURE 3 are shown in the form of current sources I1 and I2. FIGURES 4a and 4b correspond to two different states of the circuit in FIGURE 3.

[60] This circuit 32 comprises a MOS transistor M5, the source S of which is connected to the cathode C and the drain of which is connected to the MOS transistor M1. An inverter switch 36 is connected to the drain of the transistor M5 and outputs the clock signal H. The grid of the transistor M5 is connected to the output from the inverter switch 36.

[61] Also with reference to FIGURE 5, when the input E to the MOS transistor M1 changes from a high level to a low level (FIGURES 4a to 4b), the transistor M5 allows a very low current to pass, due to the delay in switching of the inverter switch 36. On the other hand, in the case in which the input changes from a low level to a high level (FIGURES 4b to 4a), the MOS transistor M5 allows a current to pass that is additional to current I1, thus enabling an

offset of the switching threshold. Thus, a hysteresis is created.

[62] The equations for the hysteresis thresholds V_{IH} and V_{IL} are defined as follows:

$$V_{IH} = Vt_n + \sqrt{\frac{I_1 + I_{2IH}}{\left(\frac{W}{L}\right)_n \cdot \frac{\mu Cox}{2}}} \qquad (1)$$

$$V_{IL} = Vt_n + \sqrt{\frac{I_1 + I_{2IL}}{\left(\frac{W}{L}\right)_n \cdot \frac{\mu Cox}{2}}} \qquad (2)$$

in which:

W/L denotes the ratio of the transistor dimensions;

Vt_n denotes the threshold voltage of the MOS;

μ denotes the mobility of the carriers; and

Cox denotes the oxide capacitance.

[63] With reference now to FIGURE 6, the count circuit is composed of a combination of three flip flops D 38, 40 and 42. This structure forms an asynchronous modulo 8 counter. With three flip-flops D, there are three outputs Q1, Q2 and Q3. These flip flops 38, 40 and 42 receive a clock signal H output from the control circuit

14, after shaping, through three inverter switches 44, 46 and 48 that are intended to accelerate the clock signal transition times. A relatively fast clock is necessary for good counting. A zeroing input R zeroes all outputs Q1, Q2 and Q3 under the control of signal UVLO2.

[64] As mentioned above, the outputs from the count circuit Q1, Q2 and Q3 will be decoded by the combinational logic circuit 18 to select the fusible elements of the network 20 and the corresponding adjustment resistances of the modulation stage 22 to adjust the global value of the resistances R_1 and R_2 of the reference voltage source.

[65] In the example embodiment considered, the fuses network comprises six fusible elements and the modulation stage 22 essentially comprises six resistances associated with the corresponding fusible elements of the network 20 and grouped in the form of two sets of three resistances, each modulating one of the resistances R_1 and R_2.

[66] Thus, the combinational logic circuit has six outputs S_1 to S_6, each selecting one of the fusible elements and one of the resistances of the modulation stage 22.

[67] FIGURES 7 and 8 show an example embodiment of the combinational logic circuit designed to generate

selection signals S1 to S6, calculated from the truth table shown in Figure 8.

[68] Thus, in this example, the signals S1, S2, S3, S4, S5 and S6 satisfy the following relations:

$$S1 = \overline{\overline{Q3}.Q2.\overline{Q1}}; \qquad S2 = \overline{\overline{Q3}.Q2.Q1}; ; \qquad S3 = \overline{Q3.\overline{Q2.Q1}} \qquad (3)$$

$$S4 = \overline{Q3.\overline{Q2}.Q1}; \qquad S5 = \overline{Q3.Q2.\overline{Q1}}; \qquad S6 = \overline{Q3.Q2.Q1} \qquad (4)$$

We will now describe the structure of the fuses network 20 used to adjust the value of resistances R_1 and R_2, with reference to FIGURES 8a, 8b and 9.

[69] FIGURES 8a shows a structure used to adjust the value of the resistance R_1, and FIGURES 8b shows a structure used to adjust the value of resistance R_2.

[70] With reference firstly to FIGURE 8a, this portion of the circuit receives inputs consisting of signals S1, S2 and S3 output from the combinational logic circuit 18. It comprises a set of three fusible elements 50, 52 and 54 and a set of control transistors, namely a PMOS transistor M6 and NMOS control transistors M7, M8 and M9. These transistors are used to select one of the fusible elements 50, 52 and 54 as a function of the signals

S1, S2 and S3 output from the logic circuit 18, and consequently to direct the voltage present on the cathode C to cause breakdown of the selected fusible element.

[71] The circuit element shown in FIGURE 8b has a similar structure and also comprises fusible elements 56, 58 and 60 associated with the NMOS control transistors M10, M11 and M12 to select one of the fusible elements 56, 58 and 60 as a function of the control signals S6, S7 and S8 output from the logic circuit 18.

[72] However, this circuit is adapted to the configuration of the resistance R_2 to be modulated, which has its potential referenced to the ground.

[73] Note that the control transistors are sized to have an equivalent resistance of about 20 ohms. In the case of the structure shown in FIGURE 8a, in the conducting state, the equivalent resistance Ron of the PMOS control transistor M6 is three times higher than the equivalent resistance of the MOS control transistors M7, M8 and M9.

[74] The equivalent resistance Ron of the transistors is given by the following relation:

$$Ron = \frac{1}{\frac{\mu Cox}{(1+\theta(V_{gs}-V_{sp}))}\cdot\frac{W}{L}(V_{gs}-V_{sp})} \qquad (5)$$

[75] Referring now to FIGURE 9, it can be seen that each fusible element is made from an NMOS transistor M13. This component has a parasite two-pole transistor which can be used to make a short circuit, which corresponds to a broken down state of the MOS transistor M13, or an open circuit, which corresponds to a non-conducting state of the MOS transistor M13.

[76] It will be noted that a resistive bridge composed of a combination of resistances R_5 and R_6 in series, is arranged between the drain and the source of transistor M13, so as to lower the breakdown voltage of this component in order to make the operation of fuses compatible with the technology used in the reference voltage source, in order to prevent deterioration of this reference voltage source.

[77] Now with reference to FIGURE 10, on which the constituents of the fuses network 20 and their control transistors M6 to M12 have been shown, the adjustment resistances R_7, R_8, R_9, R_{10}, R_{11} and R_{12} are arranged in series with a corresponding fusible element 50, 52, 54, 56, 58 and 60. The choice of the values of these resistances depends

on the global dispersion of the reference voltage and the precision to be obtained.

[78] Considering the fusible elements and the corresponding resistances to be used for adjustment of the value of the resistance R_1 (right part of the diagram in FIGURE 10), it can be seen that the resistances R_7, R_8 and R_9, each associated with a corresponding fusible element 50, 52 and 54, are each placed in parallel on the resistance R_1. Thus, the total value of the resistance R_1 can be added by adding one of the resistances R_7, R_8 or R_9 onto it in parallel, by selectively breaking down the fusible elements 50, 52 and 54.

[79] Similarly, action can be taken on the fusible elements 56, 58 and 60 to connect one of the resistances R_{10}, R_{11} and R_{12} (left part of the circuit in FIGURE 10) in parallel on resistance R_2.

[80] As it is conceived, the invention that has just been described provides a means of precisely adjusting the reference voltage output by a voltage source, precisely, without the need to use special terminals to select the fusible elements that will be used to adjust the voltage,

and therefore keeping a standard configuration for the electronic circuit provided with such an adjustment device.

[81] In this respect, it will be noted that with this invention, it is possible to obtain a precision of the supplied reference voltage of the order of 0.5% for 100% of adjusted circuits.

[82] Finally, it should be noted that the invention is not limited to the embodiment described. As mentioned above, the invention is equally applicable to any analog electronic circuit for which such an operating parameter must be precisely adjusted, such as an operational amplifier, an oscillator, a comparator, etc.

[83] Although preferred embodiments of the method and apparatus of the present invention have been illustrated in the accompanying Drawings and described in the foregoing Detailed Description, it will be understood that the invention is not limited to the embodiments disclosed, but is capable of numerous rearrangements, modifications and substitutions without departing from the spirit of the invention as set forth and defined by the following claims.